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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,919	06/07/2000	Zhiwu Liu	0325.00374	8518

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EXAMINER

WHITMORE, STACY

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 04/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/589,919

Applicant(s)

LIU, ZHIWU

Examiner

Stacy A Whitmore

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on RCE filed 1/27/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. The prior rejections of record are respectfully maintained.
3. Claims 1-2, 4-11, and 13-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchida (US Patent 5,467,304).
4. As for claims 1 and 13, Uchida taught the invention as claimed, including an apparatus comprising:
a circuit comprising [means for] a plurality of inputs configured to provide a selected device ID from a plurality of different device ID's, wherein said plurality of inputs allow said circuit to be implemented with any of said plurality of different device ID's [fig. 1, element 4 - circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; fig. 1, element 1 – package; fig. 3, elements S5, S7, S9, S11 – id codes generated; and col. 5, lines 23-30].
5. As for claim 2, Uchida taught said selected device ID comprises a soft code [fig. 7; and col. 9, lines 13-18; and col. 10, lines 23-28].
6. As for claim 4, Uchida taught wherein each of said plurality of different device ID's identifies a unique configuration of said circuit [fig. 1, fig. 2, to elements 101 and 102; fig. 7; col. 6, lines 25-30; and col. 9, lines 13-18].
7. As for claim 5, Uchida taught wherein said selected device identification ID can be reconfigured after fabrication of said apparatus [abstract; and fig. 1, fig. 2, to elements 101 and 102; fig. 7; col. 6, lines 25-30; and col. 9, lines 13-18].
8. As for claim 10, Uchida taught said plurality of inputs comprise mark options [fig. 7, inputs to the decoder, col. 9, lines 13-18; the inputs are signals which are mark options].

Art Unit: 2812

9. As for claim 11, Uchida taught said plurality of inputs comprise configuration input pins [fig. 7, inputs to the decoder, col. 9, lines 13-18; the inputs are signals are input on pins which are used to configure the circuit].

10. As for claim 14, Uchida taught a method for selecting one of a plurality of different device identifications comprising the steps of:

receiving a plurality of inputs configured to select said one of said plurality of different device IDs [fig. 1, element 4 - circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; fig. 1, element 1 – package; fig. 3, elements S5, S7, S9, S11 – id codes generated; and col. 5, lines 23-30; fig. 7, inputs to the decoder, col. 9, lines 13-18; the inputs are signals are input on pins which are used to configure the circuit];

configuring a device ID with said selected device identification (ID), wherein said plurality of inputs allow implementation of any of said plurality of different device ID [fig. 7, inputs to the decoder, col. 9, lines 13-18; the inputs are signals are input on pins which are used to configure the circuit].

11. Claims 15-19, have similar limitations as claims 2,4-5, and 10-11, and are rejected for the same reasons as cited in the rejections of claims 2,4-5, and 10-11.

12. As for claim 6, Uchida taught

a logic circuit configured to receive a plurality of inputs [fig. 7, element 3];

a multiplexer configured to receive an output of said logic circuit [col. 9, lines 12-17; and fig. 7, element 4; and

a memory element configured to receive an output of said multiplexer [fig. 7, element 5; fig. 1, element 5].

13. As for claim 7, Uchida taught the multiplexer is configured to receive an input signal and a shift signal [col. 9, lines 12-60].

14. As for claim 8, Uchida taught said logic circuit comprises a logic gate [figs. 1 and 7, element 3].

15. As for claim 9, Uchida taught said circuit is implemented with a FIFO memory [col. 9 with respect to fig. 7].

Art Unit: 2812

16. Claims 3, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) as applied to claims 1, 6, and 14 above, and further in view of Applicants Admitted Prior Art (hereinafter referred to as AAPA).

17. As for claims 3, 12, and 20, Uchida taught the invention substantially as claimed, including the apparatus and method for implementing a plurality of different device ID's as cited above in the rejections of claims 1 and 14.

Uchida did not specifically teach wherein said circuit comprises a JTAG device compliant/controller with the IEEE standard 1149.1. Uchida did disclose the IEEE standard 1149.1 with respect to Uchida's figured circuits 1 and 7].

AAPA disclosed a JTAG compliant/controller with the IEEE standard 1149.1 [pg. 1 – pg. 3, line 17, and fig. 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida and AAPA because implementing a circuit that is JTAG compliant circuit with respect to the IEEE standard 1149.1 would provide for broad use of the already existing standard in order to be compliant with many manufacturers of devices or for varied different uses of devices within an accepted and well used standard which would provide for wide range of potential uses.

18. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

Art Unit: 2812

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore

Patent Examiner

Art Unit 2812

A handwritten signature in black ink, appearing to read 'Stacy A. Whitmore', with a stylized, cursive script.

SAW

April 10, 2003